AL8259 Core
Application Note

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General Information

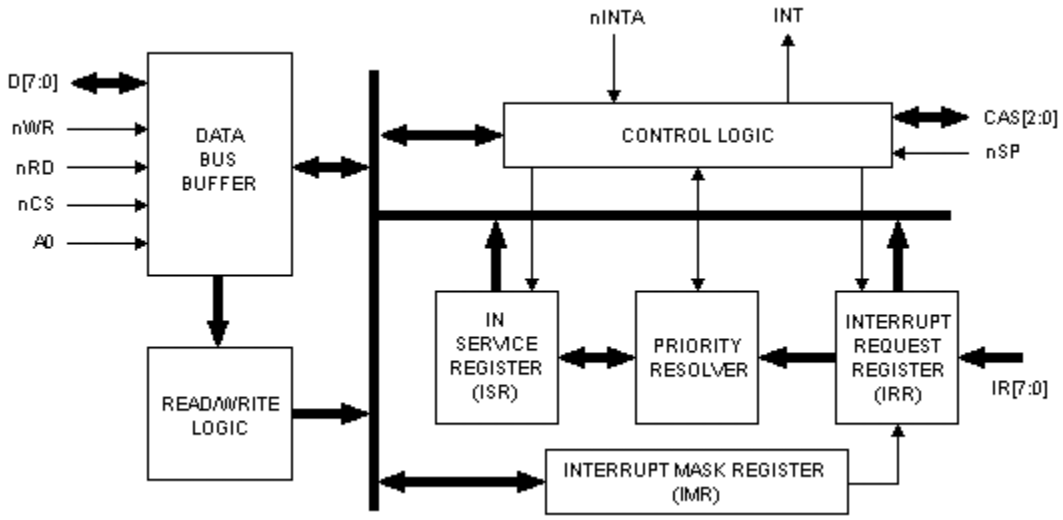
The AL8259 core is the VHDL model of the Intel™ 8259 Programmable Interrupt Controller used in Intel microprocessor systems to control and prioritize interrupts. It handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry.

Features

- Functionally based on the Intel 8259 device
- 8 Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Active High and Rising Edge Interrupt Sensitivity

Block Diagram

The basic structure of the AL8259 core is shown below:



Contents

A. Behavioral

The behavioral model is designed for the functional simulation only and it cannot be synthesized or implemented into FPGAs. The behavioral model contains the following files:

- **Pr_cell.vhd** - contains IRR and ISR registers
- **Pr_cell8.vhd** - 8 pr_cell components
- **Brl8sft.vhd** - 8-input barelshifter
- **Ipr_res.vhd** - interrupt priority resolver
- **Main.vhd** - the main block for: requesting, accepting and ending interrupts
- **AL8259.vhd** - the main block for: the control logic, read/write logic, cascade buffer logic, data bus buffer, programming words

B. Synthesizable

See the Deliverables section of this document for further details.

C. Test Vectors

See the Deliverables section of this document for further details.

Interface

The pinout of the AL8259 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the table.

Signal Name	Signal Direction	Polarity	Description
D[7:0] [1)]	INOUT	-	8-bit bidirectional data bus through which CPU reads from or writes data into the controller
CAS[2:0] [1)]	INOUT	-	Cascade lines used to cascade up to 8 Interrupt Controllers for a total capacity of 64 interrupts
IR[7:0]	IN	-	Input interrupt requests for the controller
nRD	IN	LOW	Read signal
nWR	IN	LOW	Write signal
A0	IN	-	Address signal for selection of internal registers
nCS	IN	LOW	Chip Select signal
nINTA	IN	LOW	When active low, interrupt acknowledge signal is asserted, the controller drives programmed interrupt vector onto the data bus
nSP	IN	LOW	Slave program/enable; indicates the master/slave mode operation for the controller in the non-buffered mode
INT	OUT	-	Interrupt output signal.

NOTES:

1. Each bidirectional pin is defined in the core interface as three separated VHDL ports. Optionally, using the VHDL Interface (See the Deliverables section of this document for further details), it can be merged to one bidirectional VHDL port.

Core Implementation Data

The core has been synthesized and implemented to different types of reprogrammable devices. The model has been verified using the simulation environment and tested on the real hardware.

Software				
Synthesis Tool	Synopsys FPGA Express™ build 2.1.3.3220			
Implementation Tools	Xilinx Foundation™ 2.1i SP2, Altera MAX+plusII™ 9.21, Quartus™ 1.0 A			
Verification Tool	Active-HDL™ 3.5 build 437			
Hardware				
Vendor	Xilinx		Altera	
Device Family	4K	Virtex™	FLEX™ 10K	APEX™ 20K
Target Device	XC4062XLA-9	XCV300-4	EPF10K100-1	APEX20
Area	171CLBs (7%)	coming soon	coming soon	coming soon
System Clock fmax	17MHz	coming soon	coming soon	coming soon

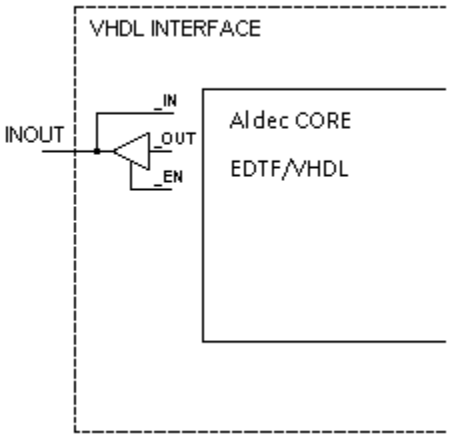
Deliverables

After you request the desired compiled synthesizable core, Aldec delivers the following files:

- Both technology-dependent EDIF (AL8259_CORE.EDN) and VHDL (AL8259_CORE.VHD) netlists
- Aldec VHDL Interface (AL8259.VHD)
- User-Guide and Application Notes
- Sample designs

Usually Aldec delivers both EDIF and VHDL netlists for customers who order the synthesizable model. The EDIF netlist is used for the place and route process and VHDL is the post-synthesis netlist used for the simulation only. Of course, both netlists are technology-dependent, because they are created after the synthesis where the customer needs to specify a vendor, target family, etc.

Aldec provides optionally a VHDL interface for its synthesizable models for these customers who need bidirectional ports in the core interface. See the picture below:



Aldec can provide also a set of VHDL test benches for their cores. Usually they are sold at the additional charge.

Source codes are sold on a case-by-case basis.